

Application No. 10/596,727

August 7, 2008

Reply to the Office Action dated May 7, 2008

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AMENDMENTS TO THE DRAWINGS:

The attached sheet of Drawings includes changes to Fig. 1. This sheet, which includes Figs. 1 and 2, replaces the original sheet including Figs. 1 and 2.

Attachment: One Replacement Sheet.

REMARKS/ARGUMENTS

Claims 7-14 are pending in this application. By this Amendment, Applicant AMENDS the Drawings.

Applicant greatly appreciates the Examiner's indication that Claim 9 would be allowable if rewritten in independent form including all of the features of the base claim and any intervening claims.

On page 2 of the outstanding Office Action, the Examiner objected to the Drawings because a portion of the circuit in **Fig. 1** near the resistive element **15** is missing. Applicant has amended **Fig. 1** to include the missing portion of the circuit. Accordingly, Applicant respectfully requests reconsideration and withdrawal of this objection to the Drawings.

On page 3 of the outstanding Office Action, the Examiner rejected Claim 7 under 35 U.S.C. § 102(b) as being anticipated by Taneji et al. (JP 08-191238), as cited in the IDS dated June 22, 2006. On page 4 of the outstanding Office Action, the Examiner rejected Claims 8 and 10 under 35 U.S.C. § 103(a) as being unpatentable over Taneji et al. On page 5 of the outstanding Office Action, the Examiner rejected Claims 11-14 under 35 U.S.C. § 103(a) as being unpatentable over Taneji et al., as applied to Claims 7 and 8 above, and further in view of Applicants Admitted Prior Art (AAPA), Figure 2.

Applicant respectfully traverses the rejections of Claims 7, 8, and 10-14.

Applicant's Claim 1 recites:

A signal output circuit comprising:
an output transistor of an NPN type bipolar transistor arranged to output an output signal;
a ground side output control transistor that turns ON and OFF according to an input signal so that turning ON drops the potential of a base of the output transistor to turn OFF the output transistor, and turning OFF raises the potential of the base of the output transistor to turn ON the output transistor;
a base current supply resistive element arranged to supply current from an input power supply to the base of the output transistor;
a power supply side output control transistor located between the base current supply resistive element and the base of the output transistor and arranged to turn ON and OFF in opposite ways as the ground side output control transistor according to the input signal;

a ground side current bypass transistor, that turns ON and OFF in the same way as the ground side output control transistor according to the input signal so that turning ON allows the current of the base current supply resistive element to flow in order to drop the voltage applied to the power supply side output control transistor and turning OFF stops the current of the base current supply resistive element from flowing; and

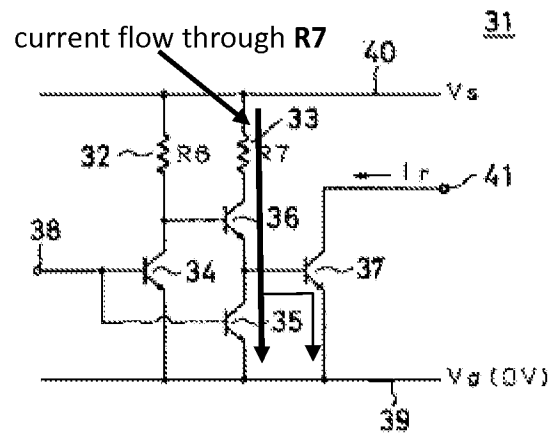
a current limitation resistive element located between the ground side current bypass transistor and the base current supply resistive element **that limits the current of the base current supply resistive element that turning ON of the ground side current bypass transistor allows to flow.** (emphasis added)

In response to the previous Office Action dated December 19, 2007, Applicant amended Claim 7 to recite the feature of “a current limitation resistive element ... that limits the current of the base current supply resistive element that turning ON of the ground side current bypass transistor allows to flow.”

In response to Applicant’s argument that Taneji et al. fails to teach this feature, in the third paragraph on page 9 of the Office Action, the Examiner alleged that **R7** of Taneji et al. (which the Examiner alleged corresponds to the base current supply resistive element recited in Claim 7) is connected to **R6** of Taneji et al. (which the Examiner alleged corresponds to the current limitation resistive element recited in Claim 7) through **Vs**.

Applicant respectfully disagrees.

No current from **R7** of Taneji et al. flows through **R6** of Taneji et al. The current that flows through **R7** of Taneji et al. flows through reference numbers **35** and **36**, with some small portion flowing through **37**. As seen in the below marked-up **Fig. 5** of Taneji et al., the current through **R7** flows from v_s (source) to v_g (ground), without flowing through **R6**. Although both **R6** and **R7** are connected to v_s , none of the current that flows through either one flows through the other. **R6** of Taneji et al. does not limit the current from **R7** of Taneji et al. That is, Taneji et al. fails to teach or suggest the feature of “a current limitation resistive element ... that limits the current of the base current supply resistive element that turning ON of the ground side current bypass transistor allows to flow” as recited in Claim 7.



Accordingly, Applicant respectfully requests reconsideration and withdrawal of the rejection of Claim 7 under 35 U.S.C. § 102(b) as being anticipated by Taneji et al.

The Examiner has relied upon AAPA to allegedly cure various deficiencies in Taneji et al. However, AAPA, applied alone or in combination with Taneji et al., fail to teach or suggest the feature of “a current limitation resistive element ... that limits the current of the base current supply resistive element that turning ON of the ground side current bypass transistor allows to flow” in combination with the other features recited in Applicant’s Claim 7.

Accordingly, Applicant respectfully submits that the prior art of record, applied alone or in combination, fails to teach or suggest the unique combination and arrangement of elements recited in Claim 7 of the present application. Claims 8-14 depend upon Claim 7 and are therefore allowable for at least the reasons that Claim 7 is allowable.

In view of the foregoing amendments and remarks, Applicant respectfully submits that this application is in condition for allowance. Favorable consideration and prompt allowance are solicited.

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The Commissioner is authorized to charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account No. 50-1353.

Respectfully submitted,

Dated: August 7, 2008

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